Unit / Module Name:	DSP Image Processing baseboard
Unit / Module Number:	AV800
Used On:	
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CONFIDENTIAL

Approvals		Date
Managing Director		
Software Manager		
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Revision History

Issue	Changes Made	Date	Initials
0.9	Initial Draft	04/01/2010	AJP
0.91	Added mechanical and connector details	11/01/2010	AJH
0.92	Change BKT part number to BKS	22/03/2010	AJH
0.93	Added mechanical mounting hole size	21/04/2010	AJH

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1 Introduction

The Av800 is a expandable DSP based processing board capable of accepting two Advanced Vision Expansion Boards (AVXBs). The board is based around the Texas Instruments TMS320DM6467 DSP.

It can either function as an intelligent display driver capable of driving most LCD panels, or it can be used as a stand alone embedded image processing system. The functionality is defined by the AVXB cards added to the system and the target software loaded onto the system.

An integrated fpga allows hardware acceleration functions to be implemented using vhdl.

The DSPs Gigabit Ethernet link has the potential to accept or transmit Ethernet images or control information to the embedded processor.

An on board SFP interface connects directly to the fpga to allow second communications channel (fibre or copper) to be added.

An on board SATA controller allows storage of programs or images.

1.1 Related Documents

Advanced Vision Expansion Boards (AVXBs) Specification.doc
TMS320DM6467 Digital Media System-on-Chip (Rev. F)
SFP transceiver specification
USB 2.0 Specification
SATA Specification

2 Functional Description

The AV800 is an embedded fpga/DSP solution for advanced image and display solutions. It is based around the Texas Instruments TMS320DM6467 media processor and the Xilinx Spartan 3 fpga.

The basic module comprises of a DSP/FPGA core with the following features :

- The dual-core architecture. ARM926EJ-S and TMS320C64x+ DSP core.
- Spartan 3 fpga.
- SFP Module Slot.
- Dual LVDS Encoder.
- 2 AVXB's.
- Ethernet 10/100/1000.
- USB 2.0 interface.
- SATA Controller.
- Audio IO capability and processing.
- Video Encoder for various CVBS/VGA output formats.

The capabilities of the AV800 can be enhanced to suit specific customer requirements using the two AVXB expansion sockets. This can allow additional modules to be fitted. Some current AVXB cards available are listed below :

AVXB Number	Name	Description
AV939	DVI IO Module	DVI Input and Output module capable of resolutions upto 1600x1200, 1920x1080i/P30
AV949	Camera Link Module	Allows a camera Link input at base, Medium and Full Rates.
AV909	Dual Composite Video IP Module	Two separate Video input channels based on the SAA7118 video decoder
AV969	16 Input CVBS PIP Mixer	Allows multiple PIP and tile functions for 16 CVBS channels with built-in motion detection capability.
AV959	ADC/DAC Module	Quad 40MSPS 12 Bit ADC, Quad 40MPS DAC 12 bit

Table 1: AVXB modules

The basic block diagram of the AV800 is shown in Figure 1.

2.1 Block Diagram

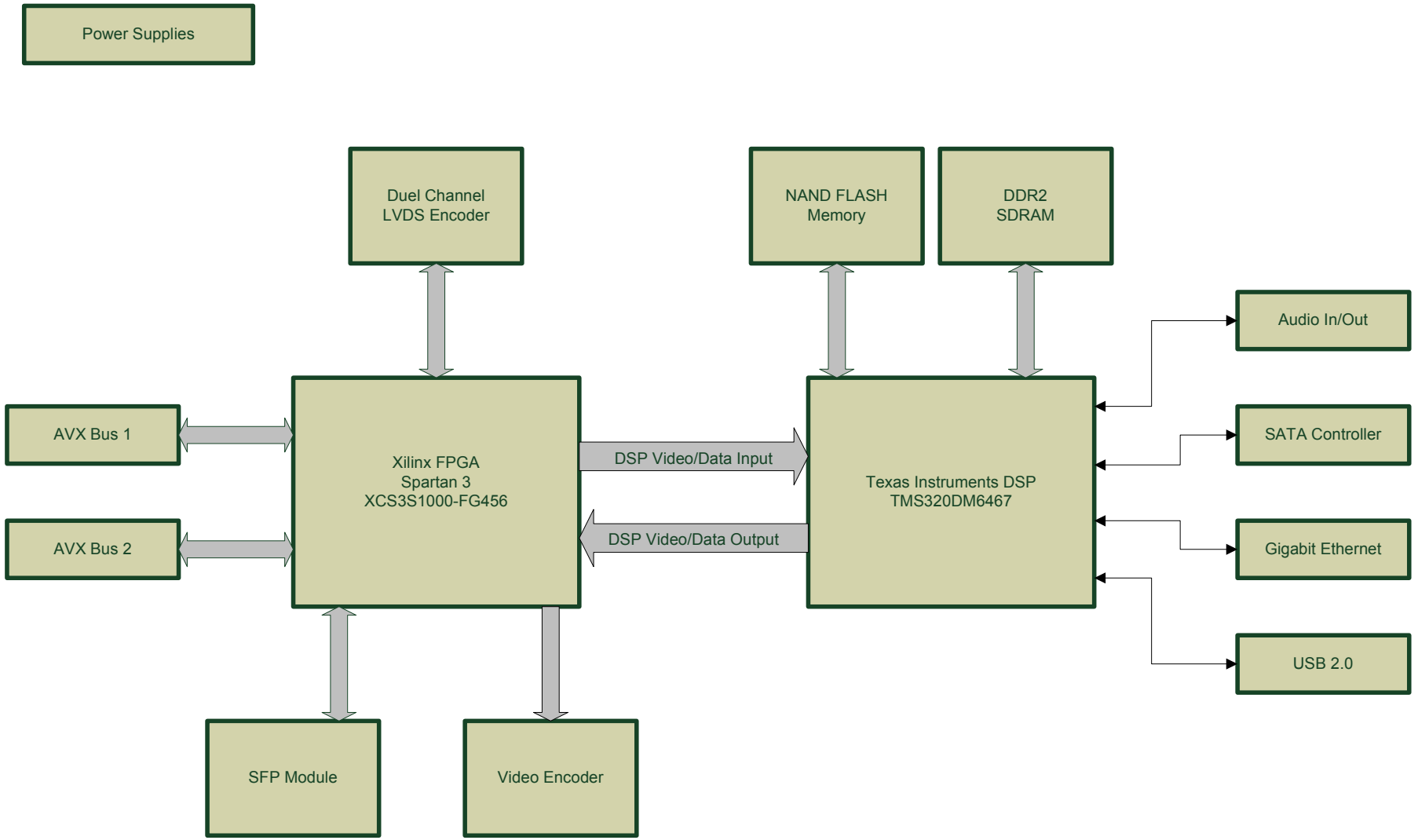


Figure 1 : Av800 Block Diagram

2.2 Module Description

This section gives a brief description of the various blocks illustrated in Figure 1.

2.2.1 Xilinx fpga

The fpga is based on the Xilinx Spartan 3 XC3S1000-FG456. It has 1920 CLB's , 120k bits of distributed RAM, 432k bits of Block RAM and 24 dedicated multipliers, making it ideal for convolution and other image processing functions. With 4 dedicated DCMs and user IOs over the AVXB's it provides a versatile solution for many different IO interfaces and standards.

2.2.2 LVDS Encoder

The encoder is based on the DS90C387 transmitter and is designed to support dual/single pixel data transmission between the fpga and Flat Panel Display up to QXGA resolutions.

The mode of the encoder is configurable via the DSP and can be used to display the DSP video port output on a flat panel LCD. With the DSP's graphical libraries, complex overlays and image mixing can be utilised create a versatile custom GUI's.

2.2.3 SFP Module

The SFP connector connects to a Texas Instruments TLK1221 Ethernet transceiver. This allows SFP modules to be fitted with transfer rates from 0.6 to 1.3 Gigabits per second. The device converts the LVPECL differential IO's into independent 10 bit Transmit and Receive interfaces which are connected to the fpga. This allows fibre and additional copper modules to be fitted.

2.2.4 AVXB interfaces

The AVX bus allows additional hardware interfaces to be connected to the AV800. There are two connectors on each AVXB, a Samtec QTH-060-01-F-D-DP-A 120 pin connector for IO and control and a 33 pin Samtec BKS-133-01-F-V-A for power. For more information on physical and electrical connectivity see the AVXB specification.

2.2.5 DSP

The main processor is based on the Texas Instruments TMS320DM6467 processor. This is a dual core processor with an ARM926EJ-S and TMS320C64x+ DSP core. This allows raw processing, such as image analysis and H.264 encode/decode to be carried out using the C64x DSP while the Arm9 can be used to run the RTOS and Ethernet/SATA control etc.

The DSP has a clock rate of 729MHz and the Arm runs off a 364.5Mhz system clocks.

For more details on the Processor see the TMS320DM6467 data sheet.

2.2.5.1 DDR Memory

The DSP has 256Mbytes of DDR2 memory for program and data storage.

2.2.5.2 FLASH Memory

A 128MByte Serial NAND FLASH holds the boot kernel for the Arm and C64x processors.

2.2.6 Audio IO

The Audio interface is based on the TLV320AIC32 low-power stereo-audio codec with a stereo headphone amplifier, as well as multiple inputs and outputs. The device is configurable via the DSP I2C bus and audio data is accessed using the SPI interface on the DSP.

2.2.7 SATA Controller

The TMS320DM6467 has a built-in ATA controller with multiword DMA and Ultra ATA 33/66/100. The AV800 utilises a Marvell 88SA8052 Serial ATA 3.0Gbs bridge so that SATA drives can be connected to the system. The device can run at 1.5Gbs as well as 3.0Gbs.

2.2.8 Ethernet

The TMS320DM6467 is capable of 10/100/1000 Mbs Ethernet transfers. The AV800 utilises the Marvel 88E1111 Gigabit Ethernet Transceiver for connection to the RJ45 connector.

2.2.9 USB 2.0 Interface

The DSP's built USB interface has a built-in PHY with USB 2.0 High/Full speed Client or USB 2.0 High/Full/Low speed Host. This allows additional storage media to be used in the system.

2.3 Interface Description

2.3.1 Mechanical Interface

The mechanical details for the panel connectors are described in this section.

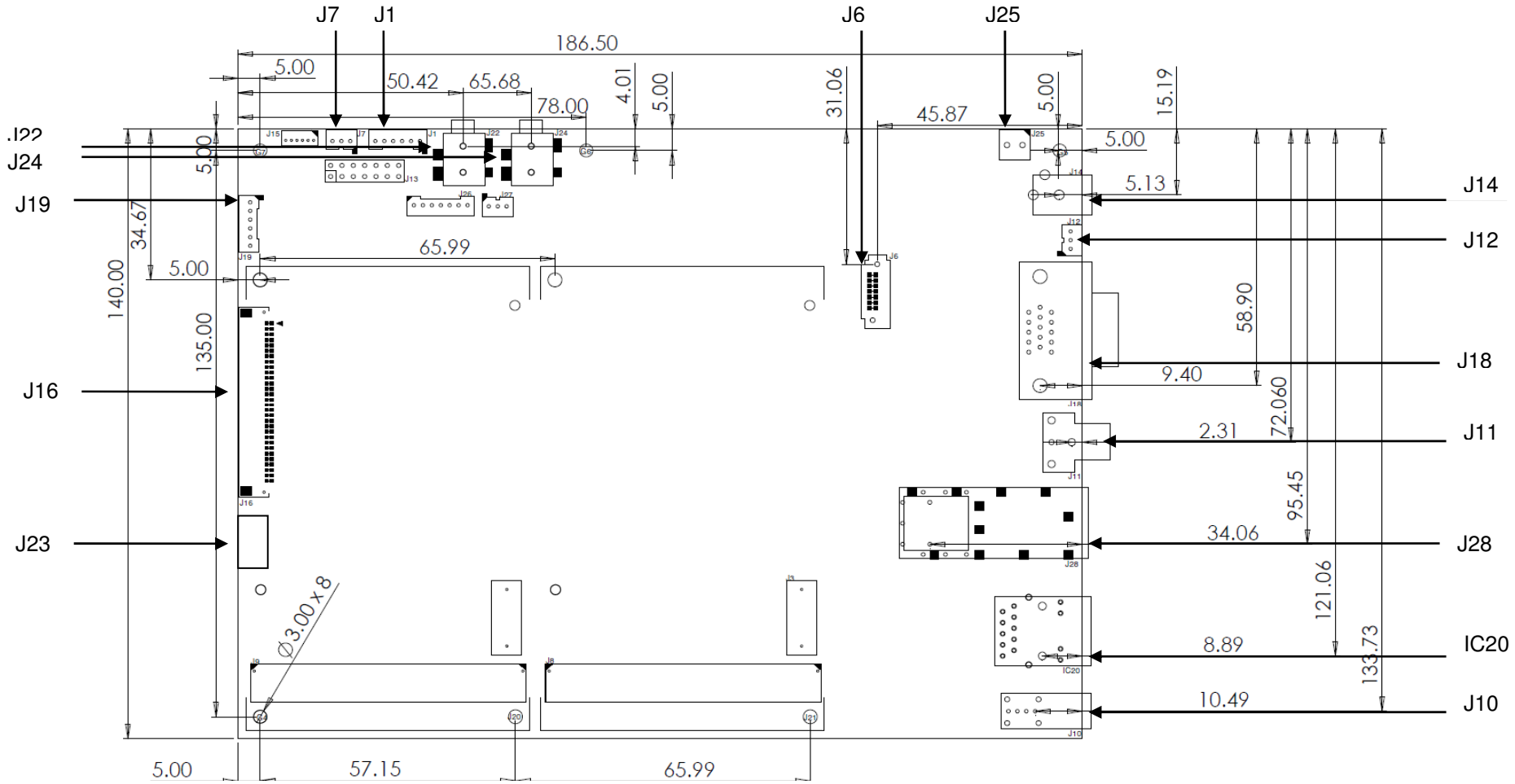


Figure 2 : Mechanical Interface

2.3.2 Electrical Interface

2.3.2.1 Power In

The unit is powered from an external 12V 3A minimum external power supply

2.3.2.2 Audio In/Out

The Audio input and output signals should not exceed 2v p/p.

2.3.2.3 SATA Connector

See the SATA specification for electrical characteristics.

2.3.2.4 Ethernet Connector

See the Ethernet specification for electrical characteristics.

2.3.2.5 USB Connector

See the USB 2.0 specification for electrical characteristics.

2.3.2.6 SFP Connector

Refer to the SFP specification for electrical details.

2.3.2.7 CVBS Connector

2.3.2.8 VGA Connector

3 Verification Procedures

The module will be tested in accordance to our QCF41 Test Procedure for the AV800.

4 Validation Procedures

The module complies with the QCF11 Certification of Conformance document for the AV800.

5 PCB Layout Details

5.1 Component Side

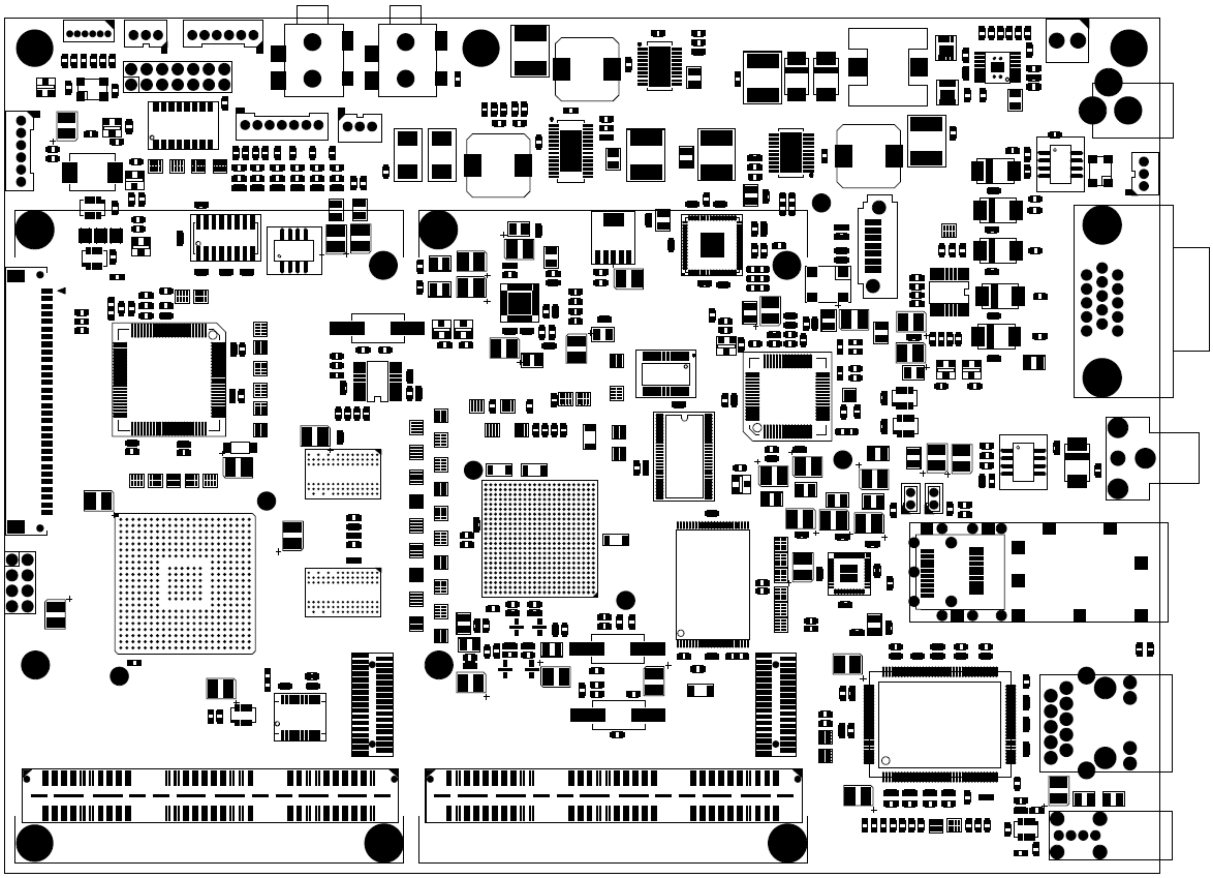


Figure 3 - PCB Layout - Top

5.2 Bottom Side

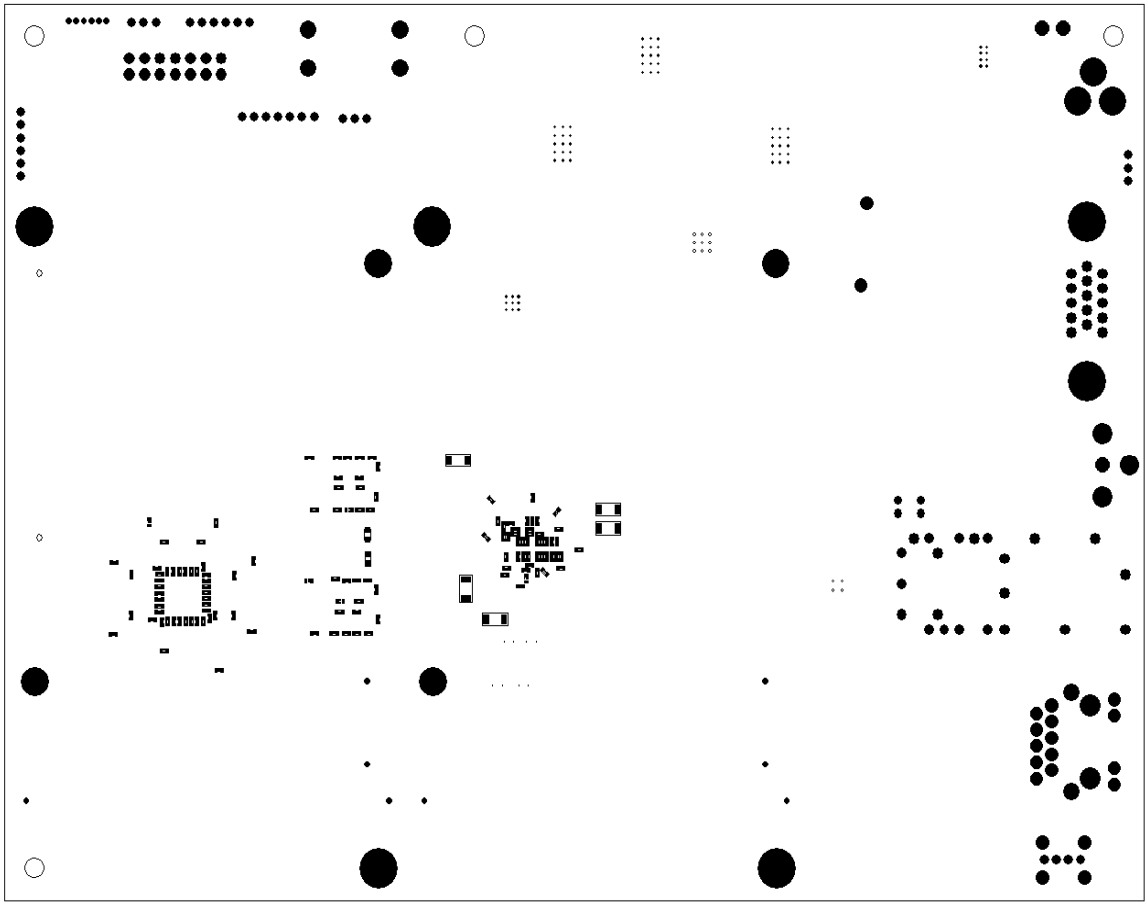
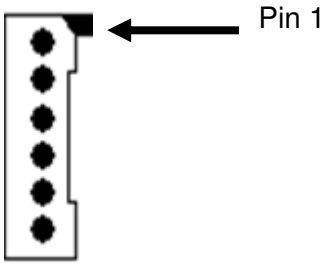


Figure 4 - PCB Layout - Bottom

6 Pinout and Package Requirements

Note:

Pin 1 on plug-in type connectors are shown by a solid shape on the silk .



6.1 AVXB Power Connector (J2/J3)

AV800 Connector Part No. BKS-133-03-F-V-A
Mating PCB Connector Samtec BKT-133-01-F-V-A

Pin #	Description	Pin #	Description
1	3.3V	2	GND
3	3.3V	4	GND
5	3.3V	6	GND
7	3.3V	8	GND
9	5V	10	GND
11	5V	12	GND
13	5V	14	GND
15	5V	16	GND
17	+12V	18	GND
19	+12V	20	GND
21	-12V[1]	22	GND
23	-12V[1]	24	GND
25	GND	26	ENU0[1]
27	ENU1[1]	28	TMS[1]
29	nTRST[1]	30	TCK[1]
31	TDI[1]	32	TDO[1]
33	NC		

Note

1. These connections are not present on the AV800.

6.2 AVXB Interface Connector (J8/J9)

AV800 Connector Part No. Samtec QTH-060-01-F-D-DP-A

Mating Connector Samtec QSH-060-01-D-DP-A

J8 – AVXB1

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	AVXB1_A00	2	AVXB1_A01	3	AVXB1_A02	4	AVXB1_A03
5	AVXB1_A04	6	AVXB1_A05	7	AVXB1_A06	8	AVXB1_A07
9	AVXB1_A08	10	AVXB1_A09	11	AVXB1_A10	12	AVXB1_A11
13	AVXB1_A12	14	AVXB1_A13	15	AVXB1_A14	16	AVXB1_A15
17	AVXB1_A16	18	AVXB1_A17	19	AVXB1_A18	20	AVXB1_A19
21	AVXB1_A20	22	AVXB1_A21	23	AVXB1_A22	24	AVXB1_A23
25	AVXB1_A24	26	AVXB1_A25	27	AVXB1_A26	28	AVXB1_A27
29	AVXB1_A28	30	AVXB1_A29	31	AVXB1_A30	32	AVXB1_A31
33	AVXB1_A32	34	AVXB1_A33	35	AVXB1_A34	36	AVXB1_A35
37	AVXB1_A36	38	AVXB1_A37	39	AVXB1_A38	40	AVXB1_A39
41	IIC_CLK	42	IIC_DATA	43	AVXB1_CTL_D00	44	AVXB1_CTL_D01
45	AVXB1_CTL_D02	46	AVXB1_CTL_D03	47	AVXB1_CTL_D04	48	AVXB1_CTL_D05
49	NC	50	NC	51	AVXB1_CTL_D06	52	AVXB1_CTL_D07
53	AVXB1_CTL_D08	54	AVXB1_CTL_D09	55	AVXB1_GCLK_A[2]	56	AVXB1_CTL_D11
57	AVXB1_CTL_D12	58	AVXB1_CTL_D13[3]	59	AVXB1_ GCLK_B[2]	60	AVXB1_CTL_D15[3]
61	AVXB1_CTL_D16	62	AVXB1_CTL_D17[3]	63	AVXB1_CTL_D18	64	AVXB1_CTL_D19[3]
65	AVXB1_CTL_D20	66	AVXB1_CTL_D21[3]	67	AVXB1_CTL_D22	68	AVXB1_CTL_D23[3]
69	AVXB1_CTL_D24	70	FPGA_VREF[1]	71	FPGA_TCK[1]	72	FPGA_TMS[1]
73	FPGA_TDI[1]	74	FPGA_TDO[1]	75	MSP_VREF[1]	76	MSP_TCK[1]
77	MSP_TMS[1]	78	MSP_TDI[1]	79	MSP_TDO[1]	80	MSP_TRST[1]
81	AVXB1_B00	82	AVXB1_B01	83	AVXB1_B02	84	AVXB1_B03
85	AVXB1_B04	86	AVXB1_B05	87	AVXB1_B06	88	AVXB1_B07
89	AVXB1_B08	90	AVXB1_B09	91	AVXB1_B10	92	AVXB1_B11
93	AVXB1_B12	94	AVXB1_B13	95	AVXB1_B14	96	AVXB1_B15
97	AVXB1_B16	98	AVXB1_B17	99	AVXB1_B18	100	AVXB1_B19
101	AVXB1_B20	102	AVXB1_B21	103	AVXB1_B22	104	AVXB1_B23
105	AVXB1_B24	106	AVXB1_B25	107	AVXB1_B26	108	AVXB1_B27
109	AVXB1_B28	110	AVXB1_B29	111	AVXB1_B30	112	AVXB1_B31
113	AVXB1_B32	114	AVXB1_B33	115	AVXB1_B34	116	AVXB1_B35
117	AVXB1_B36	118	AVXB1_B37	119	AVXB1_B38	120	AVXB1_B39

J9 – AVXB2

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	AVXB2_A00	2	AVXB2_A01	3	AVXB2_A02	4	AVXB2_A03
5	AVXB2_A04	6	AVXB2_A05	7	AVXB2_A06	8	AVXB2_A07
9	AVXB2_A08	10	AVXB2_A09	11	AVXB2_A10	12	AVXB2_A11
13	AVXB2_A12	14	AVXB2_A13	15	AVXB2_A14	16	AVXB2_A15
17	AVXB2_A16	18	AVXB2_A17	19	AVXB2_A18	20	AVXB2_A19
21	AVXB2_A20	22	AVXB2_A21	23	AVXB2_A22	24	AVXB2_A23
25	AVXB2_A24	26	AVXB2_A25	27	AVXB2_A26	28	AVXB2_A27
29	AVXB2_A28	30	AVXB2_A29	31	AVXB2_A30	32	AVXB2_A31
33	AVXB2_A32	34	AVXB2_A33	35	AVXB2_A34	36	AVXB2_A35
37	AVXB2_A36	38	AVXB2_A37	39	AVXB2_A38	40	AVXB2_A39
41	IIC_CLK	42	IIC_DATA	43	AVXB2_CTL_D00	44	AVXB2_CTL_D01
45	AVXB2_CTL_D02	46	AVXB2_CTL_D03	47	AVXB2_CTL_D04	48	AVXB2_CTL_D05
49	NC	50	NC	51	AVXB2_CTL_D06	52	AVXB2_CTL_D07
53	AVXB2_CTL_D08	54	AVXB2_CTL_D09	55	AVXB2_GCLK_A[2]	56	AVXB2_CTL_D11
57	AVXB2_CTL_D12	58	AVXB2_CTL_D13	59	AVXB2_GCLK_B[2]	60	AVXB2_CTL_D15
61	AVXB2_CTL_D16	62	AVXB2_CTL_D17	63	AVXB2_CTL_D18	64	AVXB2_CTL_D19
65	AVXB2_CTL_D20	66	AVXB2_CTL_D21	67	AVXB2_CTL_D22	68	AVXB2_CTL_D23
69	AVXB2_CTL_D24	70	FPGA_VREF[1]	71	FPGA_TCK[1]	72	FPGA_TMS[1]
73	FPGA_TDI[1]	74	FPGA_TDO[1]	75	MSP_VREF[1]	76	MSP_TCK[1]
77	MSP_TMS[1]	78	MSP_TDI[1]	79	MSP_TDO[1]	80	MSP_TRST[1]
81	AVXB2_B00	82	AVXB2_B01	83	AVXB2_B02	84	AVXB2_B03
85	AVXB2_B04	86	AVXB2_B05	87	AVXB2_B06	88	AVXB2_B07
89	AVXB2_B08	90	AVXB2_B09	91	AVXB2_B10	92	AVXB2_B11
93	AVXB2_B12	94	AVXB2_B13	95	AVXB2_B14	96	AVXB2_B15
97	AVXB2_B16	98	AVXB2_B17	99	AVXB2_B18	100	AVXB2_B19
101	AVXB2_B20	102	AVXB2_B21	103	AVXB2_B22	104	AVXB2_B23
105	AVXB2_B24	106	AVXB2_B25	107	AVXB2_B26	108	AVXB2_B27
109	AVXB2_B28	110	AVXB2_B29	111	AVXB2_B30	112	AVXB2_B31
113	AVXB2_B32	114	AVXB2_B33	115	AVXB2_B34	116	AVXB2_B35
117	AVXB2_B36	118	AVXB2_B37	119	AVXB2_B38	120	AVXB2_B39

Note

1. These connections are not present on the AV800.
2. Global clock connections on the AV800.
3. These connections are also connected to the TI DM6467 SPI interface on the AV800.
4. R203 3 way 0603 sets the voltage for the AVXB Bus Banks either 3v3 (inwards of the PCB) or 2v5.

6.2.1.1 Power In (J14, J25)

J14 – DC Jack
AV800 Connector Part No. PJ-102B

Inner Pin – 12V
Outer Pin – GND

J25 – Screw Terminal

Pin	Signal	Pin	Signal
1	GND	2	12V

6.2.1.2 LVDS Out (J16)

AV800 Connector Part No. Hirose DF14- 30P-1.25H
Mating Part No. Hirose DF14-30S-1.25C
Crimp Part No. Hirose DF14-2628SCF

Pin	Signal	Pin	Signal
1	PWR[1]	2	PWR[1]
3	PWR[1]	4	GND
5	GND	6	GND
7	GND	8	LVDS_BCLK+
9	LVDS_BCLK-	10	LVDS_B3+
11	LVDS_B3-	12	LVDS_B2+
13	LVDS_B2-	14	GND
15	LVDS_B1+	16	LVDS_B1-
17	GND	18	LVDS_B0+
19	LVDS_B0-	20	LVDS_A3+
21	LVDS_A3-	22	LVDS_ACLK+
23	LVDS_ACLK-	24	GND
25	LVDS_A2+	26	LVDS_A2-
27	LVDS_A1+	28	LVDS_A1-
29	LVDS_A0+	30	LVDS_A0-

Note:

1. PWR is jumper configurable:
   J17 - 12V Panel Supply
   J35 - 3V3 Panel Supply
   J36 - 5V Panel Supply

6.2.1.1 S-Video Out (J12)

AV800 Connector Part No. JST B-3B-PH-K-S
Mating Part No. JST PHR-3
Crimp Part No. JST SPH-002T-P0.5S

Pin	Signal	Pin	Signal
1	Luma	2	Chroma
3	GND		

6.2.1.1 VGA Out (J18)

AV800 Connector Part No. Multicomp SPC15430

Pin	Signal	Pin	Signal
1	Red	2	Green
3	Blue	4	NC
5	CAB[1]	6	GND
7	GND	8	GND
9	VCC (5V)	10	GND
11	NC	12	DDC_DATA
13	HSync	14	VSync
15	DDC_CLK	16	GND

Note

1. This connection is not present on the AV800.

6.2.1.1 Composite Out (J11)

AV800 Connector Part No. CUI RCJ-014

6.2.1.2 Backlight Inverter (J19)

AV800 Connector Part No. JST B-6B-PH-K-S
Mating Part No. JST PHR-6
Crimp Part No. JST SPH-002T-P0.5S

Pin	Signal	Pin	Signal
1	GND	2	GND
3	Brightness Ctrl	4	Inverter On/Off
5	+12v Power	6	+12v Power

6.2.1.3 RS232 Communications (J7)

AV800 Connector Part No. JST B-3B-PH-K-S
Mating Part No. JST PHR-3
Crimp Part No. JST SPH-002T-P0.5S

Pin	Signal	Pin	Signal
1	Tx	2	Rx
3	GND		

6.2.1.4 RS485 Communications (J1)

AV800 Connector Part No. JST B-6B-PH-K-S
Mating Part No. JST PHR-6
Crimp Part No. JST SPH-002T-P0.5S

Pin	Signal	Pin	Signal
1	Rx+	2	Rx-
3	GND	4	Tx+
5	Tx-	6	GND

6.2.1.5 SATA (J6)

AV800 Connector Part No. Molex 678005005

Pin	Signal	Pin	Signal
1	Tx+	2	Tx-
3	GND	4	Rx-
5	Rx+	6	GND

6.2.1.6 Ethernet (IC10)

AV800 Connector Part No. Halo Electronics HFJ11-1G16E

Pin	Signal	Pin	Signal
1	MX0+	2	MX0-
3	MX1+	4	MX1-
5	MX2+	6	MX2-
7	MX3+	8	MX3-

6.2.1.7 USB (J10)

AV800 Connector Part No. Kycon KUSBX-SLAS1N

Pin	Signal	Pin	Signal
1	VCC (5v)	2	D-
3	D+	4	GND

6.2.1.1 SFP (J28)

AV800 Connector Part No. NA (Standard SFP)

Pin	Signal	Pin	Signal
1	GND	2	Tx_Fault[1]
3	Tx_Disable	4	I2C_DATA (Mode 2)
5	I2C_CLK (Mode 1)	6	Present (Mode 3)
7	Rx_Rate[1]	8	Rx_Loss
9	GND	10	GND
11	GND	12	RD-
13	RD+	14	GND
15	VCCR	16	VCCT
17	GND	18	TD+
19	TD-	20	GND

Note

2. These connections are not present on the AV800.

6.2.1.2 Audio Line In / Mic In (J25)

AV800 Connector Part No. JST B-7B-PH-K-S
Mating Part No. JST PHR-7
Crimp Part No. JST SPH-002T-P0.5S

Pin	Signal	Pin	Signal
1	MIC_INL	2	MIC_INR
3	LINE1_INL	4	LINE1_INR
5	LINE2_INL	6	LINE2_INR
7	GND		

6.2.1.3 Audio Line Out (J27)

AV800 Connector Part No. JST B-3B-PH-K-S
Mating Part No. JST PHR-3
Crimp Part No. JST SPH-002T-P0.5S

Pin	Signal	Pin	Signal
1	LINE_OUTL	2	LINE_OUTR
3	GND		

6.2.1.4 Audio 3.5mm Stereo Mic In / (J22)

AV800 Connector Part No. CUI SJ1-3514-SMT

6.2.1.5 Audio 3.5mm Stereo Out / (J24)

AV800 Connector Part No. CUI SJ1-3514-SMT

6.2.1.1 GPIO (J23)

AV800 Connector Part No. Tyco 826953-4

Pin	Signal	Pin	Signal
1	GPIO_00	2	GPIO_01
3	GPIO_02	4	GPIO_03
5	GPIO_04	6	GPIO_05
7	GPIO_06	8	GND

7 Safety

This module presents no hazard to the user.

8 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.